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(54) A digital programmable frequency generator.

(57) Frequency generators that may be programmed are utilized in a wide variety of applications. Typical applications include radio and television receivers and transmitters, and computer devices that must operate at different clock rates, or be compatible with systems that operate at different clock rates. The present technique provides for programmably generating a frequency. A ring oscillator (201, 202, 203) receives at least one operating voltage (V_{DD}) through a programmable array (204, 210, 216) of field effect transistors (205, 206, 211, 212, 217, 218). Digitally selecting a given set of the transistors provides a given operating current for the ring, which establishes the frequency of operation. In one embodiment, the technique is implemented in a CMOS integrated circuit. This technique provides for more rapid frequency changes in a low-power circuit than can be obtained with typical prior-art techniques (e.g., a phase-locked loop).

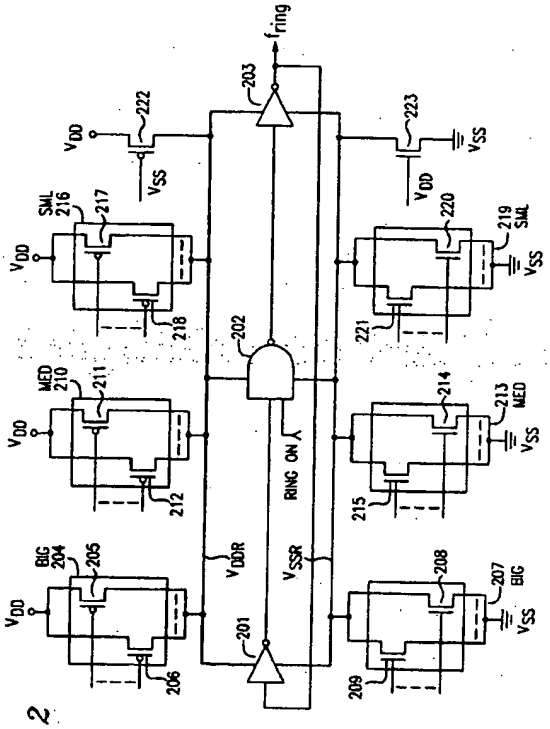

FIG. 2

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and within the desired tolerance (e.g., from 0.5% to 4% in the illustrative case), as programmed into the tolerance register 113. The tolerance/stability check circuit may be used to adapt the PFG to environmental conditions and specifications. For example, if the usage is in a high-noise system, the tolerance can be increased in value (i.e., loosened). The frequency of the ring oscillator is influenced by the programmed tolerance. For example, a looser tolerance (less accuracy) requirement allows for a lower ROSC frequency (f_{ring}), which reduces power dissipation. The stability checker sends a signal STB to the control logic 114 when the ring oscillator is stable. If a change in ring frequency is required such that a large step size transistor must be turned on/off, the stable signal is dropped to prevent any large variation in ring frequency from propagating to the output.

Frequency Divider:

The divide-by-N frequency divider 103 divides the ring oscillator output down to a lower frequency. The frequency divider 103 is typically designed so that the programmable frequency output is step-wise continuous over the entire programmable range. That is, the frequency output is quantized (for example, in steps of approximately 0.5%) over the output frequency range (for example, 20 kHz to 100 MHz). The divider 103 in the illustrative case consists of a divide by 2-or-3 followed by a chain of divide-by-2 blocks. To minimize power dissipation, the divide-by-2 chain may be a ripple counter and unneeded portions of the chain (higher order bits) are inactive. To program a desired frequency, the frequency divider 103 and reference frequency register 109 are provided with values as follows:

$$N = \frac{f_{out}}{f_{ring}},$$

where f_{out} is the desired output frequency, and f_{ring} is the frequency of the ring oscillator necessary to obtain the desired output frequency. In the illustrative case, $N = (2 \text{ or } 3) \times 2^L$, where L typically ranges from 0 to 6.

$$\text{reference frequency register} = f_{ring} \times \frac{K}{f_{ref}}$$

where K is a fixed value depending on the implementation (K=7 in the illustrative case), and f_{ref} is the frequency of the crystal oscillator 105.

Output Clock Generator:

The output clock generator 104 receives source selection information from the control logic 114 and input clock sources from the crystal oscillator and the frequency divider. It includes an input multiplexer and output formatter (not shown). The input multiplexer is designed to allow the output frequency to be switched without a glitch. To switch from the crystal oscillator 105 to the frequency divider 103, the multiplexer control signal disables the crystal oscillator signal path and enables the frequency divider path after 2 clock cycles from the frequency divider. A complementary sequence occurs when switching from the frequency divider to the crystal oscillator. The formatter is able to produce variously formatted clock outputs (e.g., 2-phase, 4-phase, etc.) In addition, this block halts the output in a predetermined state. This corresponds to the very low power stopped clock mode.

Control Logic:

The control logic 114 continuously monitors the signals within the PFG as well as the input control signals. In the power-up mode, the output clock generator 104 is instructed to use the crystal oscillator 105 as the clock. When the PFG register is updated, the control logic checks to see if the ring oscillator is required for operation. If so, the ring is turned on and the control logic waits for the frequency controller to set the stability check signal. While waiting for the stability signal to be set, the output clock generation may continue using the crystal oscillator as the source clock. When stability is achieved, the output clock generator is instructed to use the output of the frequency divider 103 as the clock source. If the control logic senses loss of stability, it instructs the output clock generator to use the crystal oscillator clock until the frequency controller once again determines that stability is achieved.

While the system shown in Fig. 1 is illustrative of a clock generator, the binary-controlled ring oscillator as shown illustratively in Fig. 2 may be used in a variety of other applications, as will be apparent to persons of skill in the art. The number of stages in the ring oscillator, and the number and grouping of transistors in the binary current tree may differ from those shown herein. Various implementations of the digital feedback loop are possible. However, the present technique may be used in applications that do not require a feedback loop nor reference frequency. Furthermore, while the above embodiment has been illustrated in CMOS technology, other technologies are possible. For example, a single conductivity type of transistor may be used to control the current flow from only a single power supply voltage, allowing for designs with only n-channel transistors in NMOS technology, or alternatively only p-channel transistors in PMOS technology, for example. Applications in bipolar technologies, including those that implement GaAs and various other device types, are also possible and included herein. In the bipolar case, the binary current tree is typically current controlled, rather than voltage controlled.

Claims

1. A system for programmably generating a range of frequencies, said system including a power supply (V_{DD}), and an integrated circuit comprising a ring oscillator (102) that includes inverters (201, 202, 203) coupled to said power supply, CHARACTERIZED IN THAT said inverters are connected to said power supply through a multiplicity of transistors (205, 206, 211, 212, 217, 218), and in that there is provided means (101) for providing binary control signals to the control terminals of said transistors to vary their conductivity between a conducting and non-conducting state, whereby the frequency of oscillation of said ring oscillator may be varied.

2. A system as claimed in claim 1 wherein said power supply is adapted to provide positive and negative voltages, and a first multiplicity of said transistors (205, 206, 211, 212, 217, 218) connects said inverters to the positive power supply voltage conductor (V_{DD}), and a second multiplicity of said transistors (208, 209, 214, 215, 220, 221) connects said inverters to the negative power supply voltage conductor (V_{SS}).

3. A system as claimed in claim 2 wherein said first multiplicity of transistors are p-channel field effect transistors, and said second multiplicity of transistors are n-channel field effect transistors.

4. A system as claimed in claim 1,2 or 3 including means (105) for providing a reference frequency, and wherein said means for providing binary control signals includes a frequency controller (108, 109, 110, 111) for comparing the frequency of said ring oscillator to said reference frequency.

5. A system as claimed in claim 4 wherein said means for providing a reference frequency includes a crystal (106) that is external to said integrated circuit.

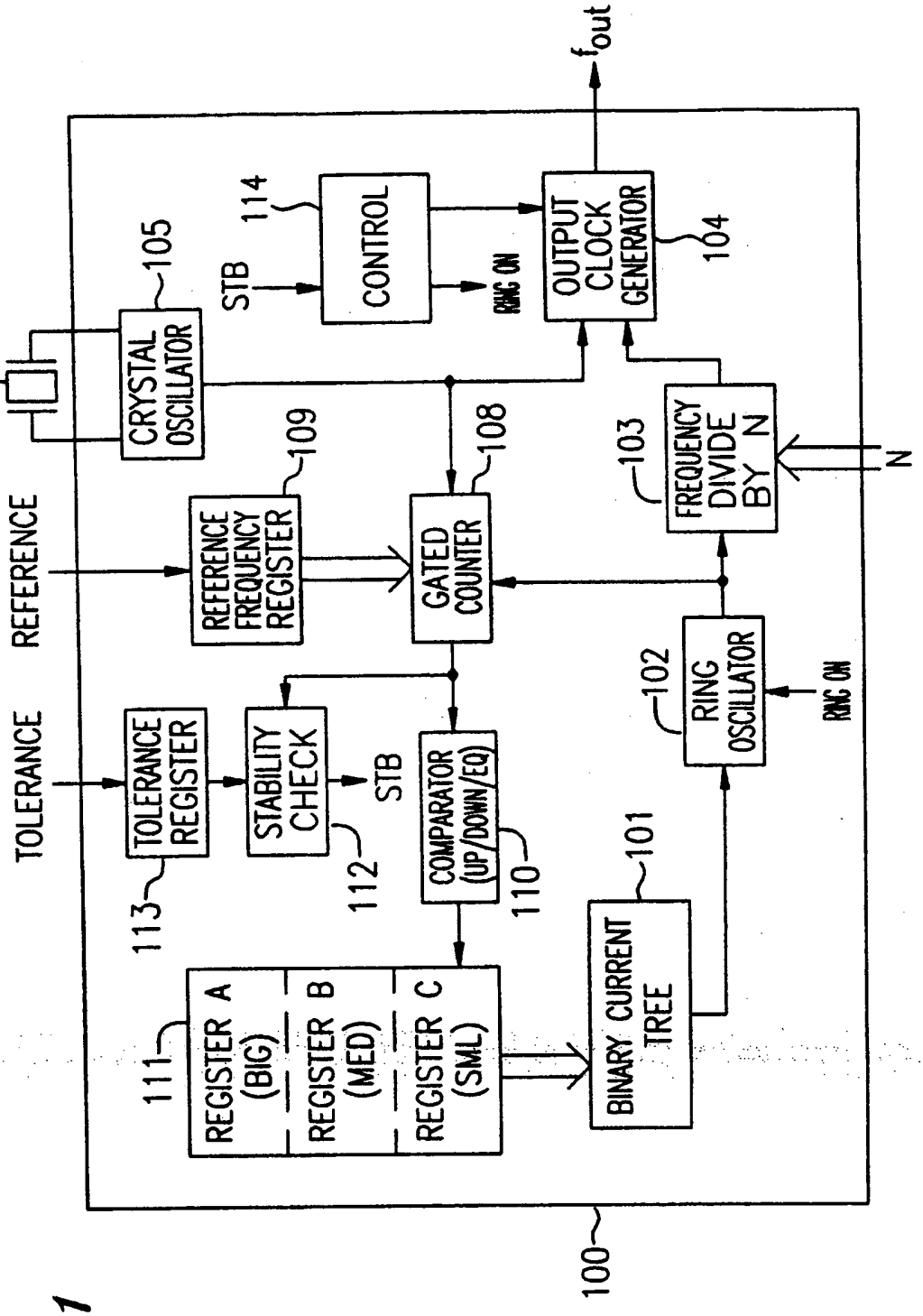
f_{out}
OUTPUT CLOCK GENERATOR
104
CONTROL
114
STB
RING ON
CRYSTAL OSCILLATOR
105
106
REFERENCE
REFERENCE FREQUENCY REGISTER
109
GATED COUNTER
108
FREQUENCY DIVIDE BY N
103
N
TOLERANCE
TOLERANCE REGISTER
113
STABILITY CHECK
112
STB
COMPARATOR (UP/DOWN/EQ)
110
RING OSCILLATOR
102
RING ON
REGISTER A (BIG)
REGISTER B (MED)
REGISTER C (SML)
111
BINARY CURRENT TREE
101
100

FIG. 1

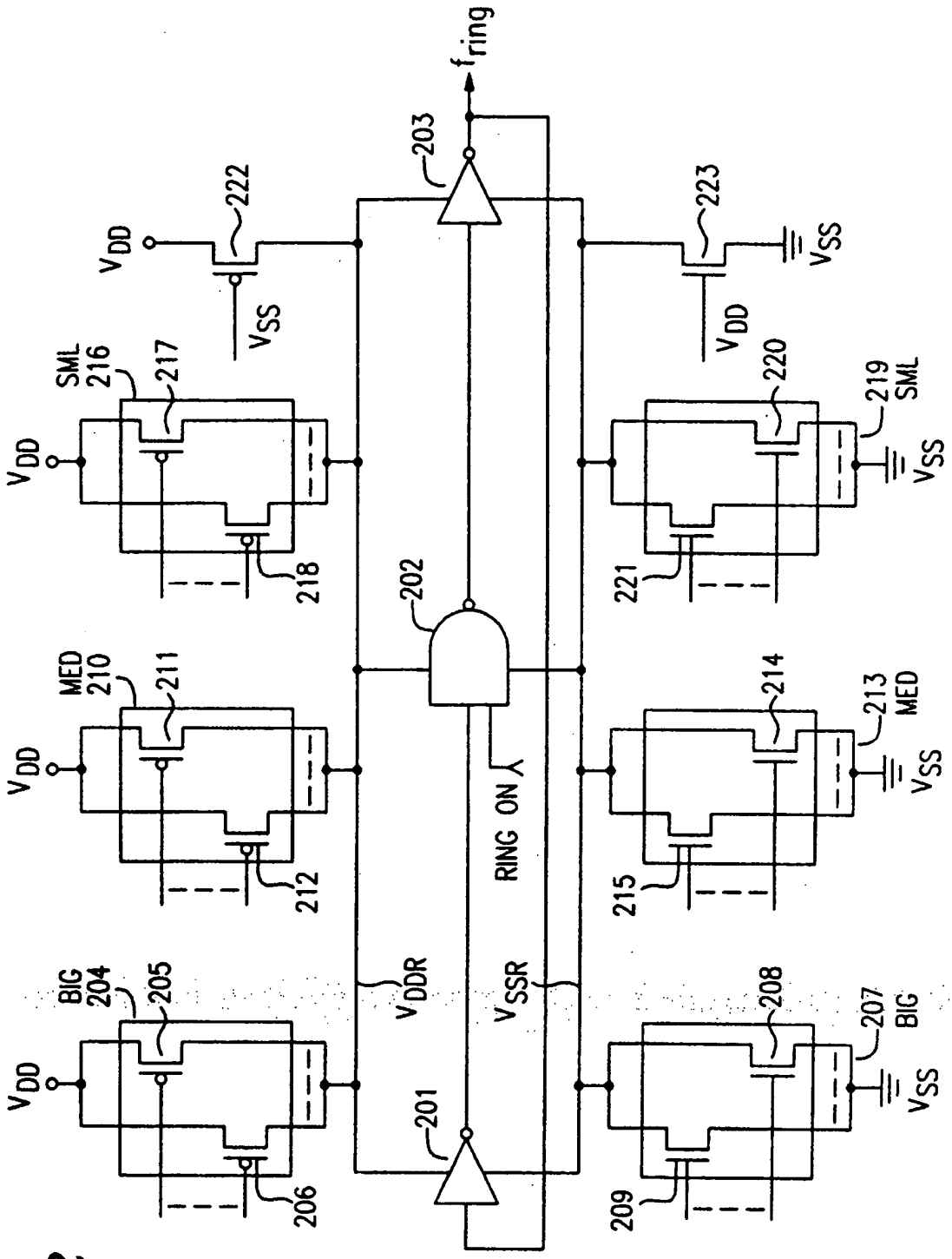
f_{ring}
203
222
223
V_{DD}
V_{SS}
SML
216
217
218
220
219
221
202
MED
210
211
212
214
213
215
RING ON
V_{DDR}
V_{SSR}
BIG
204
205
206
208
207
209
201

FIG. 2